Test & Yield Challenges of Chiplet-Based Semiconductor Products

Chetan Arvind Patil
Contributing Writer | EPDT

The semiconductor industry is fundamentally shifting how silicon (Si) chips are designed and manufactured. For decades, the primary approach when looking to increase performance and functionality was through the advancement of monolithic (aggregated) chip designs, where all the component elements were integrated into a single die. However, as the semiconductor industry approaches the limits of traditional scaling, due to economic and physical constraints, a new paradigm has now emerged - the chiplet.

At its core, a chiplet is a smaller, modular die that serves as a building block for creating complex systems. Instead of fabricating a single, massive chip, manufacturers can assemble multiple chiplets, with each of them being optimised for specific tasks. These can then be assembled into a single package.

Through this approach, greater design flexibility is enabled, with chip developers able to mix-and-match process nodes - using advanced nodes for performance-critical components and older nodes for cost-effectiveness. However, this modularity brings its own set of issues.

Integrating multiple chiplets into a cohesive system introduces complexities with regard to conducting tests and maintaining acceptable yield figures. For instance, each chiplet must be tested individually and as part of the final system. Interconnections between chiplets, typically implemented through advanced packaging technologies like die-to-die interfaces, have to be error-free to ensure reliable data transfer. Any defect in these connections can have a detrimental effect on the entire system's functionality, even if the individual chiplets themselves are perfect. Moreover, the actual assembly process introduces additional yield concerns. Combining numerous chiplets means multiplying the potential points of failure. Addressing all these problems requires rethinking of traditional design testing and manufacturing strategies.

Test challenges in chiplet-based products

The testing of chiplet-based designs introduces complexity beyond what's encountered in monolithic chips. While such monolithic chips are tested as a single unit after fabrication, chiplet-based systems require a more intricate testing approach to ensure individual chiplet functionality and seamless integration at the system level. This dual-layer testing brings forth various technical difficulties, each of which must be addressed to maintain product reliability and performance.

Key test challenges associated with chiplet-based systems will include:

- Testing individual chiplets - Chiplets can have diverse functional capabilities (e.g. analogue, RF, digital, etc.), with each requiring unique testing methodologies. Limited die area for shift-left features, like design-for-test (DFT) or built-in self-test (BIST), will complicate in-process testing. Comprehensive validation will thus be harder to attain.

- Die-to-die interconnect testing - Ensuring signal integrity across interconnects is critical, along with addressing power delivery and verifying accurate data transfer at chiplet boundaries.

- Lack of standardised test protocols - The absence of universal chiplet testing standards forces engineers to develop custom strategies, increasing resource demands and creating compatibility issues, especially with multi-vendor integration. Universal chiplet interconnect express (UCIe) is expected to solve this challenge though.

- Testing the final system - System-level testing must verify thermal performance, identify hotspots and ensure test access in dense packages. Often advanced techniques will be required here.

- Time and cost pressures - The added complexity of chiplet testing increases test time and pushes up manufacturing

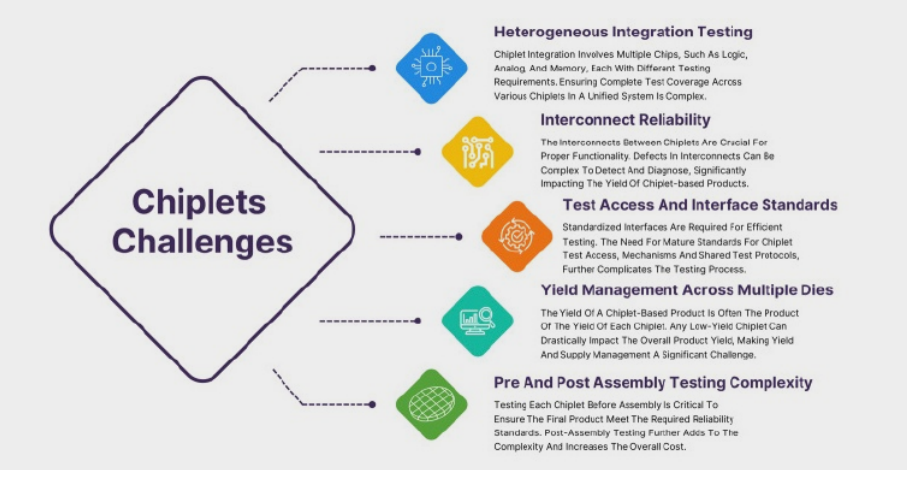

Figure 1: A summary of the issues that chiplet-based designs bring with them

costs. Having access to scalable, cost-effective methods is therefore essential, if true economic viability is to be realised.

Yield challenges in manufacturing/assembly

In chiplet-based designs, achieving high yields becomes exponentially more difficult, due to the modular and interconnected nature of this approach. Unlike monolithic chips, whose yield will be tied to a single fabrication process, chiplet-based products require consistent quality across multiple fabrication, assembly and integration steps. The following list gives a detailed breakdown of the specific yield challenges that are unique to chiplet-based semiconductor products. They are:

- Yield loss in individual chiplets - Advanced nodes typically have lower yields, due to their variability, with added defect risks from integrating diverse functionalities.
- Assembly-induced defects - Defects in interconnects and misalignment during bonding can cause failures, while material stresses from thermal expansion may lead to cracks or delamination occurring.
- Cumulative yield loss in the system - As the number of chiplets increases, overall yield may drop due to system-level testing. Defective chiplets also waste assembly resources if not identified early on.
- Thermal and reliability concerns - Uneven thermal distribution can create hotspots and reduce reliability, while thermal cycling might result in package-level failures.
- Economic implications of low yield - Yield loss raises up production costs and will consequently hit companies' profit margins. Mitigation strategies like redundancy and defect analytics driven by artificial intelligence (AI) can help to improve overall yield.

The future of chiplet-based product development

The next decade is set to witness transformative advancements in test methodologies and yield optimisation for chiplet-based designs - driven by the adoption of industry standards like UCIe and the emergence of next-generation packaging technologies developed explicitly for chiplet use. These standards will play a pivotal role in addressing the unique challenges of chiplet integration, including variability across process nodes, interconnect defects, operational reliability and cumulative yield losses from the combining of multiple chiplets within a single package.

As chiplet adoption scales upwards, smaller companies and start-ups are also poised to drive innovation in test automation and yield enhancement tools by building solutions that are aligned with the aforementioned standards. Simultaneously, government and academic partnerships will accelerate research into advanced tools, chiplet-inspired testing techniques and process optimisations - thus strengthening the supporting ecosystem. By embedding universal standards into test and yield strategies, the semiconductor industry can achieve excellent chiplet-driven reliability, cost efficiency and scalability.