Factors Affecting Semiconductor Node Selection

Chetan Arvind Patil
Contributing Writer | EPDT

Deciding on the optimal process node is an essential element of semiconductor design. This is especially true for the development of application-specific integrated circuits (ASICs) and system-on-chip (SoC) devices. It will have implications in relation to operational performance, power efficiency, the area taken up, the unit cost, etc.

As semiconductor technology has continued to progress, nodes have shrunk from 180nm in the early 2000s to the 3nm implementations now being employed in certain high-end processors and memories. As a consequence, heightened transistor densities, accelerated speeds, plus lower power consumption characteristics can be attaiåned.

Transitioning to an advanced node is not necessarily the best route to take though. As a result, design engineers need to thoroughly evaluate their specific situations. They must be fully aware of the numerous technical and commercial trade-offs involved, before making a final decision.

Knowing your nodes

Traditionally, the node figure referred to the transistor gate length. Still, modern node names now encompass multiple process optimisations beyond feature size. These include metal pitch scaling, contact efficiency and new transistor architectures.

Among the key technology transitions that have taken place in recent years are:

- 180nm to 65nm - This saw the introduction of copper interconnects, replacing aluminium, to attain better performance.
- 45nm to 28nm - The introduction of high-k metal gate (HKMG) technology has reduced leakage and improved power efficiency.
- Emergence of 16nm/14nm - Via transition from planar transåistors to FinFETs, dramatic improvements in performance and power efficiency have been witnessed.
- Moving to 7nm and below - Extreme ultra-violet lithography (EUV) becomes necessary to print more minor features.
- 3nm/sub-3nm - Adoption of gate-all-around FETs (GAAFET) and stacked nanosheet transistors, thereby enabling further scaling.

Each transition increases manufacturing complexity and cost, requiring companies to strategically evaluate whether a given node justifies its investment - thus making semiconductor node selection a key step in product development.

Node selection considerations

The choice of a semiconductor node significantly influences a product's performance, cost structure and time-to-market. In a competitive landscape where efficiency, pricing and innovation drive success, companies must carefully assess whether migrating to an advanced node justifies the investment or if leveraging a mature node provides better returns. A well-chosen node can determine whether a company leads in performance or struggles with cost overruns.

Table 1 gives a summary of all the trade-offs across performance, cost, manufacturing complexity and time-to-market. Different industry sectors prioritise semiconductor nodes based on a balance of various parameters. While cutting-edge nodes (5nm and below) enable high-performance artificial intelligence (AI) processing, 5G communication and data centre applications, many industries still rely on mature nodes (28nm, 40nm and 65nm) for cost-effectiveness, power savings and extended lifecycle support.

Consumer electronics devices, such as wearables and smart home gadgets, benefit from 28nm and 40nm nodes, where lower power consumption and affordability take precedence over raw performance. On the other hand, automotive and industrial applications require long-term reliability and strict safety certifications - making 16nm to 28nm a preferred range, due to well-established process stability and supply chain availability.

For smartphones and edge AI, 7nm and 5nm nodes dominate, offering optimised power efficiency, AI acceleration and support for 5G connectivity. These

Factor	Ultra-Advanced Nodes	Mature Nodes
Transistor density	Higher density, enabling better computational power for AI, 5G and HPC.	Lower transistor density, sufficient for automotive and industrial applications.
Power efficiency	Lower operating voltage, but leakage increases below 7nm, with power savings diminishing.	More power-efficient at lower clock speeds, making them highly suitable for battery-powered and energy-sensitive applications.
Performance scaling	Support higher clock speeds, AI acceleration and parallel processing.	Sufficient for applications where performance is secondary to efficiency.
Wafer costs	$9k to $16k+ per wafer due to EUV lithography and complex fabrication.	$0.7k to $4k per wafer, providing cost-effective production.
Design costs	Design cost increases from ~$50M to over $250M.	Lower non-recurring engineering (NRE) costs and widely available design libraries, reducing upfront investment.
Electronic design automation (EDA) and intellectual property (IP) related costs	Require newer EDA tools, optimised IP and extensive validation. All adding to associated costs.	Mature design ecosystem with proven IP availability, plus lower risks.
Yield stability	Lower initial yield, leading to higher cost per functioning chip.	Stable manufacturing yields, reducing cost per chip.
Manufacturing options	Only TSMC, Samsung and Intel manufacture below 5nm, leading to foundry capacity constraints.	More foundry options, including GlobalFoundries, UMC and SMIC, offering higher supply chain flexibility.
Lithography complexity	7nm and below require EUV lithography, significantly increasing fab investment and lead time.	Use of deep ultra-violet (DUV) lithography, which is cheaper and widely available.
Geopolitical issues	Heavily affected by trade regulations, impacting supply chain security and fab access.	More resilient supply chain, with diversified manufacturing hubs.
Time-to-market	2-3 years to stabilise, requiring early adoption risk-taking.	Faster time-to-market, leveraging proven, mature manufacturing processes.
Market adoption	Selected players push leading-edge nodes for competitive advantage in premium segments.	Automotive and industrial players favour mature nodes for cost savings and reliability.

Table 1: The most prominent semiconductor node trade-offs

nodes balance performance and battery life, which is crucial for mobile devices. High-performance computing (HPC) and AI processors push the limits further, leveraging 5nm, 4nm and even 3nm to maximise computational density and parallel processing capabilities.

Meanwhile, medical, avionics and industrial automation sectors prioritise older nodes (such as 65nm and 40nm) for radiation tolerance, ongoing operational stability and cost-effectiveness. The embedded systems and microcontroller units (MCUs) found in industrial control hardware and legacy automotive applications often remain at 90nm or above, where cost and simplicity outweigh the need for aggressive scaling.

Ultimately, node selection is driven by industry-specific needs, rather than a race toward the smallest feature size. While AI and HPC demand cutting-edge nodes, most semiconductor applications still depend on mature nodes to strike the right balance of cost, power efficiency and reliability.

Conclusion

Semiconductor node selection will be dependent on the particular performance, cost and market/commercial requirements associated with a design project. In addition to node scaling, supply chain constraints and geopolitical factors will also need to be taken into account. Looking ahead, semiconductor innovation will go beyond traditional node scaling - with chiplets, advanced packaging, 3D stacking and new transistor architectures all helping to bring future generations of microelectronic devices into existence.